## REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

**Claim Amendment**

Claim 1 is amended such that the sliced signal has a first binary value and a second binary value according to the result of comparison, and the sliced signal keeps at the first binary value for a first time period and keeps at the second binary value for a second time period. Also, the limitation "***for detecting the phase at which the transition of the sliced signal occurs, based on a reference clock***" is replaced with ***"detecting a relation between the first time period and the second time period "***.

Please refer to paragraphs [0031] to [0037] of the present invention, which disclose the detailed operations of the phase detector 370. Briefly, the phase detector 370 includes at least D flip-flop series 510 and at least transition phase detecting device 530. The D flip-flop series 510 output 0 or 1 corresponding to the transition of the sliced signal Xo3 (Paragraph [0031]). Also, the phase detecting device 530 can determine the upward transition phase and the downward transition phase of the sliced signal Xo3 (Paragraph [0033]). Also, the transition phase detecting device 530 can compute the upward transition phase and the downward transition phase of the sliced signal Xo3, and thereby the relation between the first time period for the first level V1 (i.e. the first binary value ) and the second time period for the second level V2 (i.e. the first binary value ) is detected (Paragraph [0037]).

In addition, due to the amendments made to claim 1, claim 2 is amended accordingly.

The applicant believes that no new matter is introduced. Consideration of above-identified amendments is respectfully requested.

**Claim Rejections – 35 USC 103 (a)**

Claims 1-2, 12-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popplewell et al. (US 6304071) in view of Yamamoto (US 6057730) further in view of Chong et al. (US 7200769). Specifically, claims 1-2, 12-13 and 15-17 are rejected under 35 U.S.C. 103(a) due to the same reasons as which in the First Office Action at 2007/10/05

**Response**

**Claim 1**

On page 3 and page 4 of the Final Office Action at 2008/04/02, the examiner states that Popplewell teaches the limitation "***for detecting the phase at which the transition of the sliced signal occurs, based on a reference clock***". However, as above-mentioned, claim 1 is amended such that the sliced signal has a first binary value and a second binary value according to the result of comparison, and the sliced signal keeps at the first binary value for a first time period and keeps at the second binary value for a second time period. Also, the limitation "***for detecting the phase at which the transition of the sliced signal occurs, based on a reference clock***" is replaced with ***"detecting a relation between the first time period and the second time period "***, and the phase error detector 5 of Popplewell is used for providing a phase error value (column 3, line 32). Also, the phase error is determined according to Yn-1, Xn-2, Xn-1, Xn (Fig 3). Therefore, the phase error detector 5 of Popplewell can not reach the function of ***"detecting a relation between the first time period and the second time period "*** thus Popplewell fails to teach the limitation of claim 1 of the

present invention.

Additionally, on page 3 and page 4 of the Final Office Action at 2008/04/02, the examiner states that Chong teaches the limitation "***for detecting the phase at which the transition of the sliced signal occurs, based on a reference clock***". As above-mentioned description, the limitation "***for detecting the phase at which the transition of the sliced signal occurs, based on a reference clock***" is replaced with ***"detecting a relation between the first time period and the second time period "***. However, the phase detector 350 taught by Chong is utilized for determining whether a rising edge of the system clock precedes a rising edge of the delayed clock (column 6, lines 24~26), and can not read on the function of ***"detecting a relation between the first time period and the second time period,"*** thus Chong fails to teach the limitation of claim 1 of the present invention.

Additionally, Yamamoto discloses a clock recovery circuit, which compares two sample values, selects a small one thereof, and controls the sampling clock signal so that the amplitude of the smaller one is minimized (column 1 line 61 to column 2, lines 16). Therefore, Yamamoto only discloses comparing two sampled values and improves the signal sampling but fails to teach or suggest ***"detecting a relation between the first time period and the second time period,"*** in claim 1 of the applicant's disclosure.

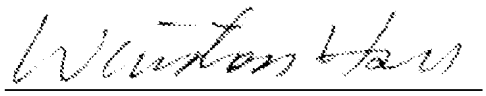
Claims 2 and 10-17 are dependent upon claim 1, and should be allowed if claim 1 is found allowable.

**Conclusion**

Based on the above remarks/arguments, the applicant respectfully submits that all of the rejections set forth in the Office Action dated 04/02/2008 have been overcome and the pending claims are now in condition for allowance. The applicant therefore respectfully requests that a timely Notice of Allowance be issued in this case. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact the undersigned applicant's representative at the

number indicated below.

Sincerely yours,



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